RICOH

R3116x Series

AEC-Q100 Compliant

0.8% Low Voltage Detector with Output Delay for Automotive Applications

No. EC-161-171011

OUTLINE

The R3116x is a CMOS-based voltage detector IC with high detector threshold accuracy and ultra-low supply current, which can be operated at an extremely low voltage and is used for system reset as an example.

This IC consists of a voltage reference unit, a comparator, resistors for detector threshold setting, an output driver, a hysteresis circuit and an output delay circuit. The detector threshold is internally fixed with high accuracy (±12mV: $-V_{DET}$ < 1.5V, ±0.8%: $-V_{DET} \geq$ 1.5V) and does not require any adjustment. The release output delay time is adjustable by the capacitor connected to the CD pin.

Two output types, Nch open drain type and CMOS type are available.

In addition to SOT-23-5 package, an ultra-small DFN1212-4 package are also available for high-density mounting.

FEATURES

- Operating Voltage Range (Maximum Rating) .... 0.5V to 6.0V (7.0V)
- Operating Temperature Range .... −40°C to 105°C
- Supply Current .... Typ. 0.35µA ($-V_{DET}$=1.5V, V_{DD}=$-V_{DET}$+1V)
- Detector Threshold Range .... 0.7V to 5.0V (0.1V steps)
- Detector Threshold Accuracy .... ±0.8% ($-V_{DET} \geq$ 1.5V)
- Temperature-Drift Coefficient of Detector Threshold .... Typ. ±30ppm/°C
- Built-in Output Delay Circuit .... Typ. 100ms with an external capacitor: 0.022µF
- Output Delay Time Accuracy .... ±15% ($-V_{DET} \geq$ 1.5V)
- Output Types .... Nch Open Drain and CMOS
- Packages DFN1212-4, SOT-23-5

APPLICATIONS

- Voltage monitoring for car accessories including car audios, car navigation systems, ETC systems.

SELECTION GUIDE

The package type, the detector threshold, the output type and the taping type for the ICs can be selected at the users' request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3116Lxx1∗-TR-#	DFN1212-4	3,000 pcs	Yes	Yes
R3116Nxx1∗-TR-#E	SOT-23-5	3,000 pcs	Yes	Yes

xx : The set detector threshold (-V_{SET}) can be designated in the range from 0.7V(07) to 5.0V(50) in 0.1V steps.

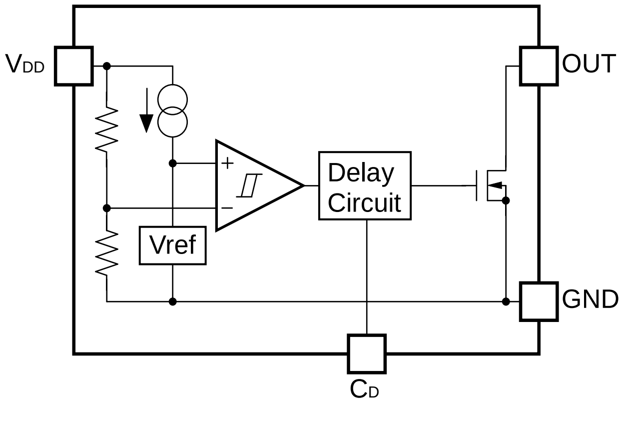
∗ : Designation of Output Type
(A) Nch Open Drain
(C) CMOS

: Quality Class

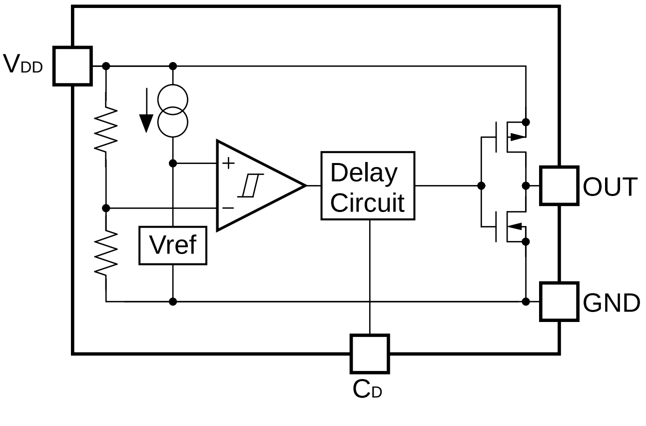
	Operating Temperature Range	Test Temperature	AEC-Q100
A	−40°C to 105°C	25°C, High	Grade 2

BLOCK DIAGRAMS

Nch Open Drain Output (R3116xxx1A)



CMOS Output (R3116xxx1C)



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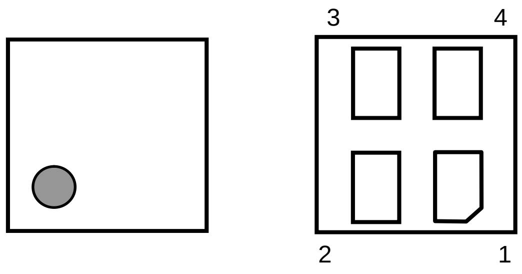
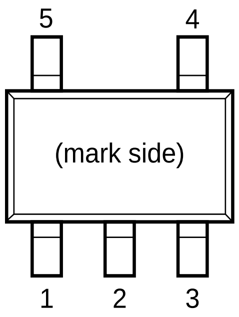
PIN DESCRIPTIONS

• DFN1212-4

Top View / Bottom View



• SOT-23-5



• **DFN1212-4**

Pin No.	Symbol	Description
1	OUT	Output Pin ("L" at detection)
2	C_D	Pin for External Capacitor (for setting output delay)
3	GND	Ground Pin
4	V_{DD}	Input Pin

• **SOT-23-5**

Pin No.	Symbol	Description
1	OUT	Output Pin ("L" at detection)
2	V_{DD}	Input Pin
3	GND	Ground Pin
4	NC	No Connection
5	C_D	Pin for External Capacitor (for setting output delay)

ABSOLUTE MAXIMUM RATINGS

Symbol	Item		Rating	Unit
V_{DD}	Supply Voltage		7.0	V
V_{OUT}	Output Voltage (Nch Open Drain Output)		V_{SS}–0.3 to 7.0	V
	Output Voltage (CMOS Output)		V_{SS}–0.3 to V_{DD}+0.3	
I_{OUT}	Output Current		20	mA
P_D	Power Dissipation* (JEDEC STD. 51-7 Test Land Pattern)	DFN1212-4	455	mW
		SOT-23-5	660	
Tj	Junction Temperature Range		–40 to 125	°C
Tstg	Storage Temperature Range		–55 to 125	°C

* Please refer to *POWER DISSIPATION* for detailed information.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{DD}	Operating Voltage	0.55 to 6.0	V
Ta	Operating Temperature Range	–40 to 105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R3116xxx1A/C (Ta=25°C)

Symbol	Item	Conditions			Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	Ta=25°C	1.5V < $-V_{DET}$ ≤ 5.0V		$-V_{DET}$ × 0.992		$-V_{DET}$ ×1.008	V
			0.7V ≤ $-V_{DET}$ ≤ 1.5V		-12		+12	mV
		−40°C ≤ Ta ≤ 105°C	1.5V < $-V_{DET}$ ≤ 5.0V		[$-V_{DET}$ ×0.985]		[$-V_{DET}$ ×1.015]	V
			0.7V ≤ $-V_{DET}$ ≤ 1.5V		[-22.5]		[+22.5]	mV
V_{HYS}	Detector Threshold Hysteresis				[$-V_{DET}$ × 0.04]		[$-V_{DET}$ × 0.07]	V
I_{SS}	Supply Current	V_{DD}= $-V_{DET}$ −0.1V	0.7V ≤ $-V_{DET}$ < 1.6V				[1.400]	μA
			1.6V ≤ $-V_{DET}$ < 3.1V				[1.500]	
			3.1V ≤ $-V_{DET}$ < 4.1V				[1.600]	
			4.1V ≤ $-V_{DET}$ ≤ 5.0V				[1.700]	
		V_{DD}= $-V_{DET}$ +1.0V	0.7V ≤ $-V_{DET}$ < 1.6V				[1.200]	
			1.6V ≤ $-V_{DET}$ < 3.1V				[1.200]	
			3.1V ≤ $-V_{DET}$ < 4.1V				[1.300]	
			4.1V ≤ $-V_{DET}$ ≤ 5.0V				[1.400]	
V_{DDL}	Minimum Operating Voltage*1	Ta=25°C					0.50	V
		−40°C ≤ Ta ≤ 105°C					[0.55]	
I_{OUT}	Output Current (Driver Output Pin)	Nch	V_{DD}=0.55V, V_{DS}=0.05V		[7]			μA
			0.7V ≤ $-V_{DET}$ < 1.1V	V_{DD}=0.6V V_{DS}=0.5V	[0.020]			mA
			1.1V ≤ $-V_{DET}$ < 1.6V	V_{DD}=1.0V V_{DS}=0.5V	[0.400]			
			1.6V ≤ $-V_{DET}$ < 3.1V	V_{DD}=1.5V V_{DS}=0.5V	[1.000]			
			3.1V ≤ $-V_{DET}$ ≤ 5.0V	V_{DD}=3.0V V_{DS}=0.5V	[2.400]			
		Pch*2	0.7V ≤ $-V_{DET}$ < 4.0V	V_{DD}=4.5V V_{DS}=−2.1V	[0.650]			mA
			4.0V ≤ $-V_{DET}$ ≤ 5.0V	V_{DD}=6.0V V_{DS}=−2.1V	[0.900]			
I_{LEAK}	Nch Driver Leakage Current*3	V_{DD}=6.0V, V_{DS}=7.0V					[80]	nA
t_D	Output Delay Time	C_D=0.022μF, V_{DD}=$-V_{DET}$−0.1V to $-V_{DET}$x1.1V	Ta=25°C	0.7V≤ $-V_{DET}$ < 1.5V	80	100	130	ms
				1.5V≤ $-V_{DET}$ ≤5.0V	85		115	
			−40°C ≤ Ta ≤ 105°C	0.7V≤ $-V_{DET}$ < 1.5V	[70]	100	[150]	
				1.5V≤ $-V_{DET}$ ≤5.0V	[75]		[135]	

All of unit are tested and specified under load conditions such that Tj≈Ta=25°C

*1 Minimum operating voltage means the value of input voltage when output voltage maintains 0.1V or less.
(In case of Nch Open Drain Output type, the output pin is pulled up with a resistance of 470kΩ to 5.0V)

*2 In case of CMOS type

*3 In case of Nch Open Drain type

● Electrical Characteristics by Detector Threshold

R3116x071A/C to R3116x501A/C

Bold values are checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C, unless otherwise noted.

(Ta=25°C)

Part Number	Detector Threshold1		Detector Threshold2		Detector Threshold Hysteresis		Supply Current1		Supply Current2		Max. Op. Voltage	Min. Op. Voltage
	$-V_{DET1}$ [V]		$-V_{DET2}$ [V]		V_{HYS} [V]		I_{SS1} [μA]		I_{SS2} [μA]		V_{DDH} [V]	V_{DDL} [V]
	Min.	Max.	Min.	Max.	Min.	Max.	Cond.	Max.	Cond.	Max.	Max.	Max.
R3116x071A/C	0.688	0.712	**0.678**	**0.723**	**0.028**	**0.049**	V_{DD}= $-V_{DET}$ -0.1V	**1.400**	V_{DD}= $-V_{DET}$ +1.0V	**1.200**	**6**	0.50 **0.55** *Note1
R3116x081A/C	0.788	0.812	**0.778**	**0.823**	**0.032**	**0.056**						
R3116x091A/C	0.888	0.912	**0.878**	**0.923**	**0.036**	**0.063**						
R3116x101A/C	0.988	1.012	**0.978**	**1.023**	**0.040**	**0.070**						
R3116x111A/C	1.088	1.112	**1.078**	**1.123**	**0.044**	**0.077**						
R3116x121A/C	1.188	1.212	**1.178**	**1.223**	**0.048**	**0.084**						
R3116x131A/C	1.288	1.312	**1.278**	**1.323**	**0.052**	**0.091**						
R3116x141A/C	1.388	1.412	**1.378**	**1.423**	**0.056**	**0.098**						
R3116x151A/C	1.488	1.512	**1.478**	**1.523**	**0.060**	**0.105**						
R3116x161A/C	1.587	1.613	**1.576**	**1.624**	**0.064**	**0.112**		**1.500**				
R3116x171A/C	1.686	1.714	**1.675**	**1.726**	**0.068**	**0.119**						
R3116x181A/C	1.786	1.814	**1.773**	**1.827**	**0.072**	**0.126**						
R3116x191A/C	1.885	1.915	**1.872**	**1.929**	**0.076**	**0.133**						
R3116x201A/C	1.984	2.016	**1.970**	**2.030**	**0.080**	**0.140**						
R3116x211A/C	2.083	2.117	**2.069**	**2.132**	**0.084**	**0.147**						
R3116x221A/C	2.182	2.218	**2.167**	**2.233**	**0.088**	**0.154**						
R3116x231A/C	2.282	2.318	**2.266**	**2.335**	**0.092**	**0.161**						
R3116x241A/C	2.381	2.419	**2.364**	**2.436**	**0.096**	**0.168**						
R3116x251A/C	2.480	2.520	**2.463**	**2.538**	**0.100**	**0.175**						
R3116x261A/C	2.579	2.621	**2.561**	**2.639**	**0.104**	**0.182**						
R3116x271A/C	2.678	2.722	**2.660**	**2.741**	**0.108**	**0.189**						
R3116x281A/C	2.778	2.822	**2.758**	**2.842**	**0.112**	**0.196**						
R3116x291A/C	2.877	2.923	**2.857**	**2.944**	**0.116**	**0.203**						
R3116x301A/C	2.976	3.024	**2.955**	**3.045**	**0.120**	**0.210**						
R3116x311A/C	3.075	3.125	**3.054**	**3.147**	**0.124**	**0.217**		**1.600**		**1.300**		
R3116x321A/C	3.174	3.226	**3.152**	**3.248**	**0.128**	**0.224**						
R3116x331A/C	3.274	3.326	**3.251**	**3.350**	**0.132**	**0.231**						
R3116x341A/C	3.373	3.427	**3.349**	**3.451**	**0.136**	**0.238**						
R3116x351A/C	3.472	3.528	**3.448**	**3.553**	**0.140**	**0.245**						
R3116x361A/C	3.571	3.629	**3.546**	**3.654**	**0.144**	**0.252**						
R3116x371A/C	3.670	3.730	**3.645**	**3.756**	**0.148**	**0.259**						
R3116x381A/C	3.770	3.830	**3.743**	**3.857**	**0.152**	**0.266**						
R3116x391A/C	3.869	3.931	**3.842**	**3.959**	**0.156**	**0.273**						
R3116x401A/C	3.968	4.032	**3.940**	**4.060**	**0.160**	**0.280**						
R3116x411A/C	4.067	4.133	**4.039**	**4.162**	**0.164**	**0.287**		**1.700**		**1.400**		
R3116x421A/C	4.166	4.234	**4.137**	**4.263**	**0.168**	**0.294**						
R3116x431A/C	4.266	4.334	**4.236**	**4.365**	**0.172**	**0.301**						
R3116x441A/C	4.365	4.435	**4.334**	**4.466**	**0.176**	**0.308**						
R3116x451A/C	4.464	4.536	**4.433**	**4.568**	**0.180**	**0.315**						
R3116x461A/C	4.563	4.637	**4.531**	**4.669**	**0.184**	**0.322**						
R3116x471A/C	4.662	4.738	**4.630**	**4.771**	**0.188**	**0.329**						
R3116x481A/C	4.762	4.838	**4.728**	**4.872**	**0.192**	**0.336**						
R3116x491A/C	4.861	4.939	**4.827**	**4.974**	**0.196**	**0.343**						
R3116x501A/C	4.960	5.040	**4.925**	**5.075**	**0.200**	**0.350**						

*Note1) V_{DD} value when output voltage is equal or less than 0.1V. In the case of Nch Open Drain output type, the output pin is pulled up to 5.0V through 470kΩ resistor.

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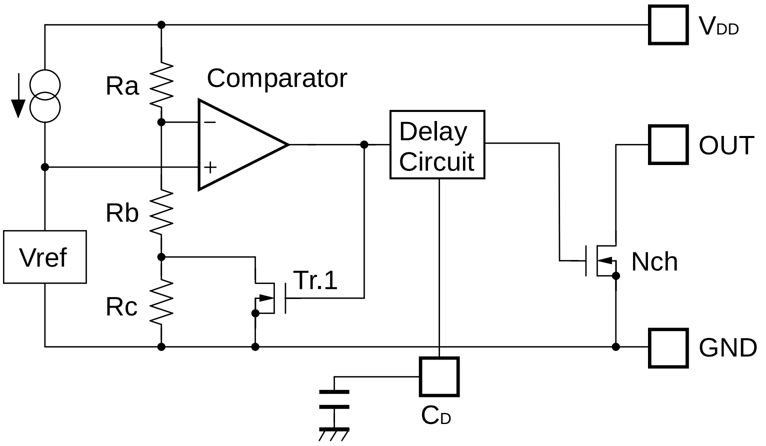
Nch Driver Output Current1		Nch Driver Output Current2		Pch Driver Output Current		Nch Driver Leakage Current		Detector Threshold Temperature Coefficient	Output Delay Time		
I_{OUT1} [μA]		I_{OUT2} [mA]		I_{OUT3} [mA]		I_{LEAK} [nA]		Δ-$V_{DET}/\Delta Ta$ [ppm/°C]	t_D [ms]		
Cond.	Min.	Cond.	Min.	Cond.	Min.	Cond.	Max.	Typ.	Cond.	Min.	Max.
V_{DD}= 0.55V V_{DS}= 0.05V	7	V_{DD}= 0.6V V_{DS}= 0.5V	0.020	V_{DD}= 4.5V V_{DS}= -2.1V	0.650	V_{DD}= 6.0V V_{DS}= 7.0V	80	±30	C_D= 0.022μF V_{DD}= $-V_{DET}$ -0.1V ↓ $-V_{DET}$ ×1.1V *Note2	80 70	130 150
		V_{DD}= 1.0V V_{DS}= 0.5V	0.400								
		V_{DD}= 1.5V V_{DS}= 0.5V	1.000							85 75	115 135
		V_{DD}= 3.0V V_{DS}= 0.5V	2.400	V_{DD}= 6.0V V_{DS}= -2.1V	0.900						

*Note2) 1. In the case of CMOS output type:
When the voltage is forced from ($-V_{DET}$)–0.1V to ($-V_{DET}$)×1.1V pulse voltage is added to V_{DD}, time interval that the output voltage reaches (($-V_{DET}$)×1.1V)/2.

2. In the case of Nch Open Drain output type:
The output pin is pulled up to 5.0V through 470kΩ, and when the voltage is forced from ($-V_{DET}$)–0.1V to ($-V_{DET}$)×1.1V pulse voltage is added to V_{DD}, time interval that the output voltage reaches 2.5V.

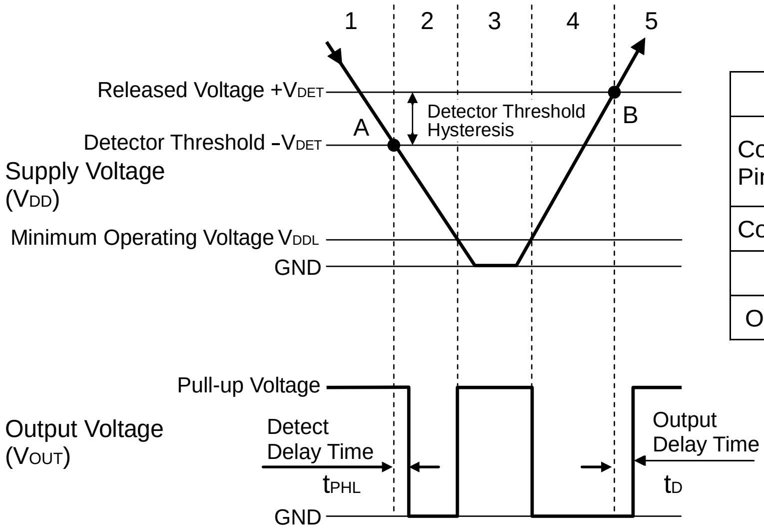
THEORY OF OPERATION

- **Operation of R3116xxx1A**



OUT pin should be pulled-up to V_{DD} or an external voltage level.

Block Diagram (R3116xxx1A)



Step		1	2	3	4	5
Comparator (−) Pin Input Voltage		I	II	II	II	I
Comparator Output		L	H	Indefinite	H	L
Tr.1		OFF	ON	Indefinite	ON	OFF
Output Tr.	Nch	OFF	ON	Indefinite	ON	OFF

I $\dfrac{Rb+Rc}{Ra+Rb+Rc} \times V_{DD}$

II $\dfrac{Rb}{Ra+Rb} \times V_{DD}$

Operation Diagram

- **Explanation of operation**

Step 1. The output voltage is equal to the pull-up voltage.

Step 2. At Point "A", Vref ≧ V_{DD}×(Rb+Rc)/(Ra+Rb+Rc) is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage ($-V_{DET}$).

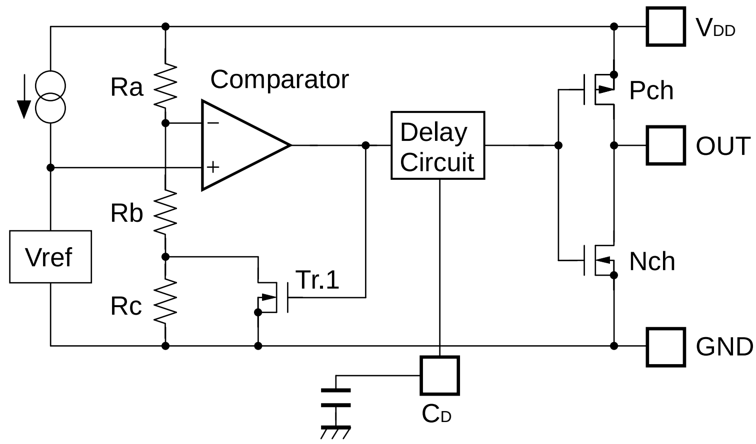
Step 3. When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite. The output voltage is equal to the pull-up voltage.

Step 4. The output voltage is equal to the GND level.

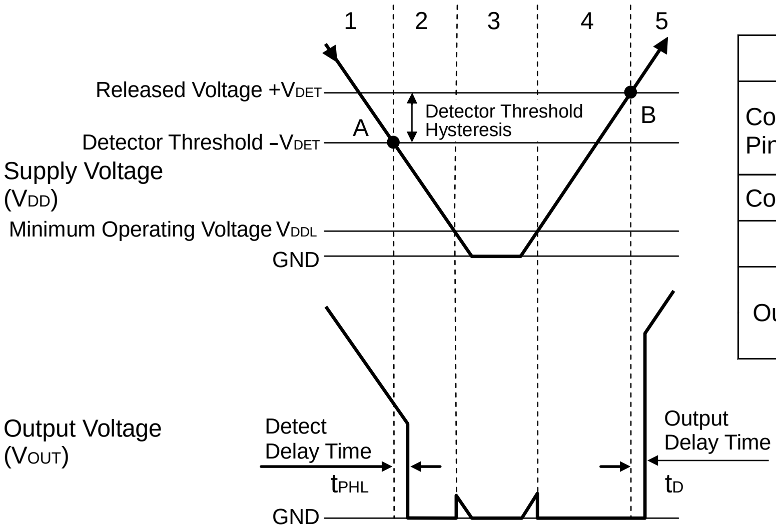
Step 5. At Point "B", Vref ≦ V_{DD}×Rb/(Ra+Rb) is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the pull-up voltage. The voltage level of Point B means a released voltage ($+V_{DET}$).

∗) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

● Operation of R3116xxx1C



Block Diagram (R3116xxx1C)



Step		1	2	3	4	5
Comparator (–) Pin Input Voltage		I	II	II	II	I
Comparator Output		L	H	Indefinite	H	L
Tr.1		OFF	ON	Indefinite	ON	OFF
Output Tr.	Pch	ON	OFF	Indefinite	OFF	ON
	Nch	OFF	ON	Indefinite	ON	OFF

I $\frac{Rb+Rc}{Ra+Rb+Rc} \times V_{DD}$

II $\frac{Rb}{Ra+Rb} \times V_{DD}$

Operation Diagram

● Explanation of operation

Step 1. The output voltage is equal to the supply voltage (V_{DD}).

Step 2. At Point "A", Vref ≧ V_{DD}×(Rb+Rc)/(Ra+Rb+Rc) is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage ($-V_{DET}$).

Step 3. When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite.

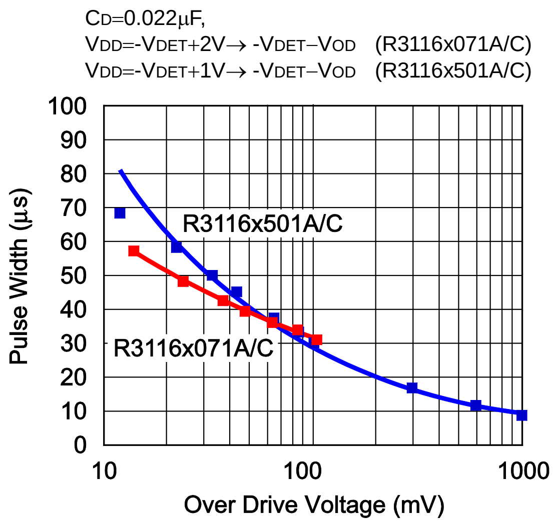
Step 4. The output voltage is equal to the GND level.

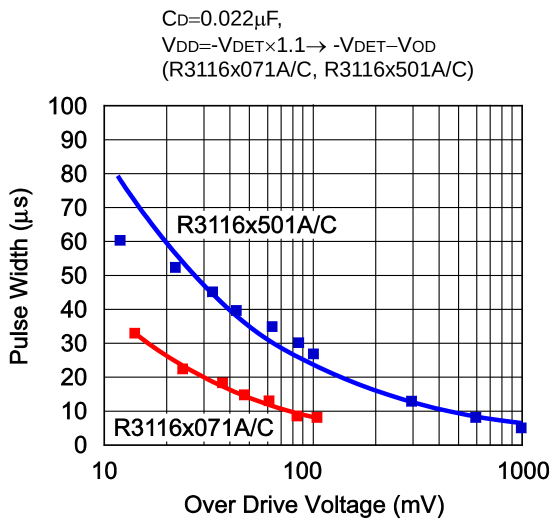
Step 5. At Point "B", Vref ≦ V_{DD}×Rb/(Ra+Rb) is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the supply voltage (V_{DD}). The voltage level of Point B means a released voltage ($+V_{DET}$).

∗) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

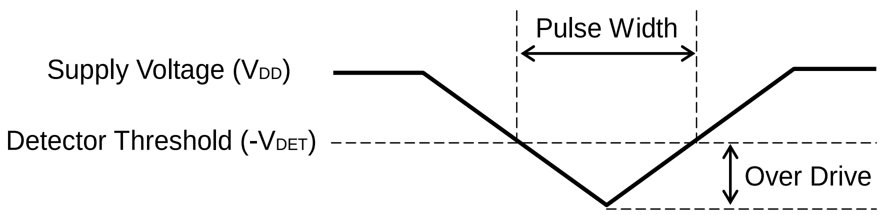
- **Detector Operation vs. Glitch Input Voltage to The VDD Pin**

When the R3116x is at released, if the pulse voltage which the detector threshold or lower voltage, the graph below means that the relation between pulse width and the amplitude of the swing to keep the released state for the R3116x.





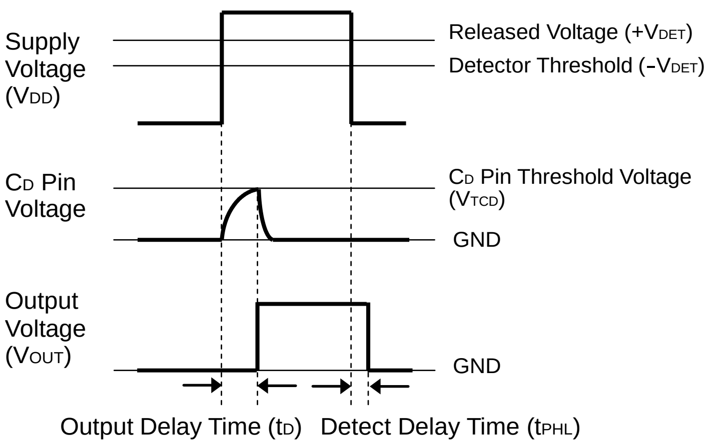
∗VOD: Over Drive Voltage



VDD Input Waveform

This graph shows the maximum pulse conditions to keep the released voltage. If the pulse with larger amplitude or wider width than the graph above is input to VDD pin, the reset signal may be output.

● Timing Chart



When the supply voltage, which is higher than released voltage, is forced to V_{DD} pin, charge to an external capacitor starts, then C_D pin voltage increases. Until the C_D pin voltage reaches to C_D pin threshold voltage, output voltage maintains "L". When the C_D pin voltage becomes higher than C_D pin threshold voltage, output voltage is reversed from "L" to "H". Where the time interval between the rising edge of supply voltage and output voltage reverse point means output delay time.

When the output voltage reverses from "L" to "H", the external capacitor starts to discharge. Therefore, when lower voltage than the detector threshold voltage is forced to V_{DD} pin, the output voltage reverses from "H" to "L" thus the detect delay time is constant not being affected by the external capacitor.

Output Delay Time

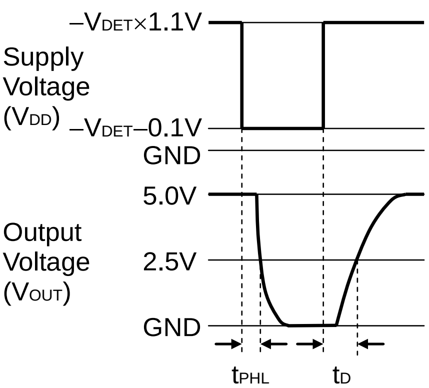
Output Delay Time (t_D) can be calculated with the next formula using the external capacitor:

$t_D(s) = 4.5 \times 10^6 \times C_D(F)$

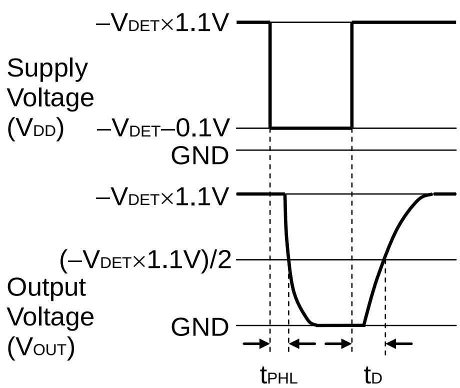
● Definition of Output Delay Time

Output Delay Time (t_D) is defined as follows:

1. In the case of Nch Open Drain Output:
   Under the condition of the output pin (OUT) is pulled up through a resistor of 470kΩ to 5V, the time interval between the rising edge of V_{DD} pulse from $(-V_{DET})-0.1V$ to $(-V_{DET})\times1.1V$ pulse voltage is supplied, the becoming of the output voltage to 2.5V.
2. In the case of CMOS Output:
   The time interval between the rising edge of V_{DD} pulse from $(-V_{DET})-0.1V$ to $(-V_{DET})\times1.1V$ pulse voltage is supplied, the becoming of the output voltage to $((-V_{DET})\times1.1V)/2$.



Nch Open Drain Output
(R3116xxx1A)



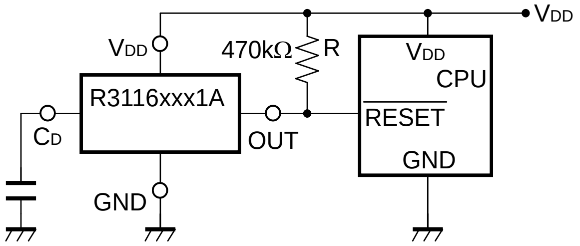
CMOS Output
(R3116xxx1C)

APPLICATION INFORMATION

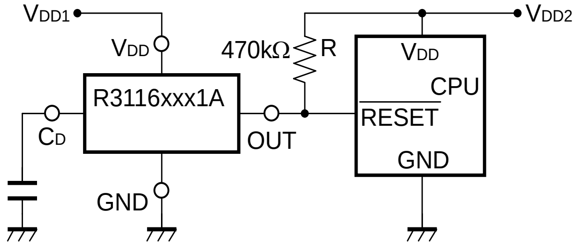
• Typical Application

R3116xxx1A CPU Reset Circuit 1 (Nch Open Drain Output)

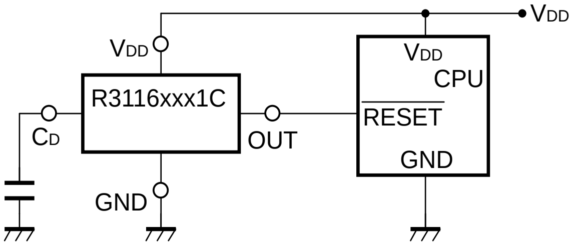
Case1. Input Voltage to R3116xxx1A is equal to Input Voltage to CPU



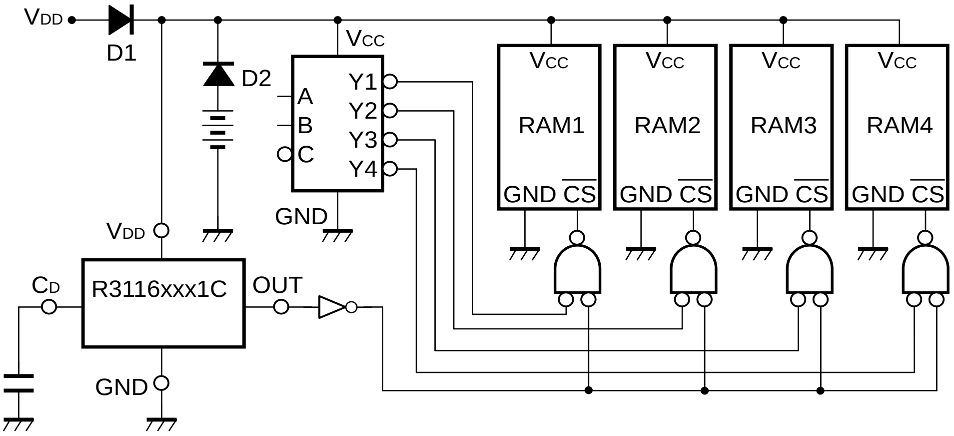
Case2. Input Voltage to R3116xxx1A is unequal to Input Voltage to CPU



R3116xxx1C CPU Reset Circuit 2 (CMOS Output)

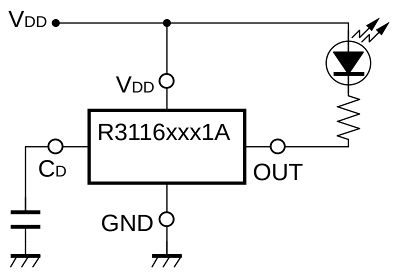


Memory Back-up Circuit

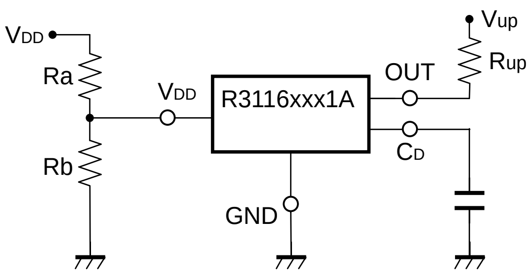


RICOH

Voltage level Indicator Circuit (lighted when the power runs out) (Nch Open Drain Output)



Detector Threshold Adjustable Circuit 1 (Nch Open Drain Output)

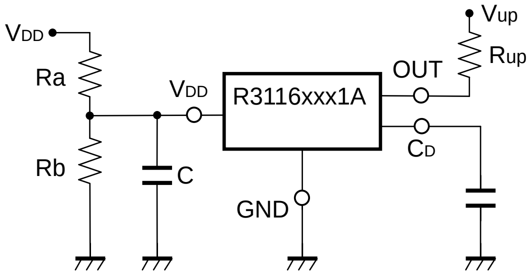


Adjustable Detector Threshold=(-V_{DET})×(Ra+Rb)/Rb

Hysteresis Voltage=(V_{HYS})×(Ra+Rb)/Rb

∗1) To prevent oscillation, set Ra ≦ 1kΩ, Rb ≦ 100Ω.
∗2) If the value of Ra is set excessively large, voltage drop may occur caused by the supply current of IC itself, and detector threshold and hysteresis voltage may vary.
∗3) If Vup and V_{DD} are connected, the voltage dropdown caused by Rup, may cause difference in the hysteresis voltage.

Detector Threshold Adjustable Circuit 2 (Nch Open Drain Output)

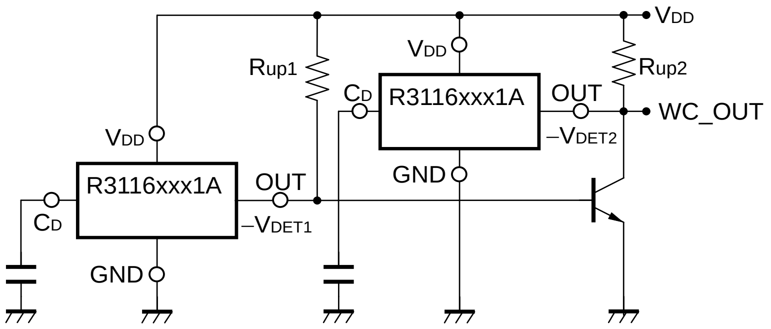


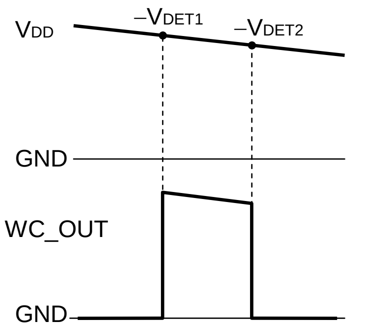
Adjustable Detector Threshold=(-V_{DET})×(Ra+Rb)/Rb

Hysteresis Voltage=(V_{HYS})×(Ra+Rb)/Rb

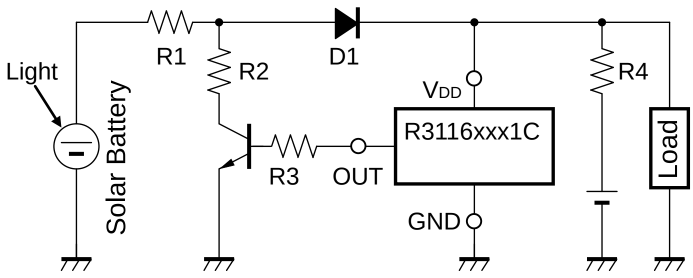
∗1) To prevent oscillation, set Ra ≦ 10kΩ, Rb ≦ 1kΩ, C ≧ 1µF.
∗2) If the value of Ra is set excessively large, voltage drop may occur caused by the supply current of IC itself, and detector threshold and hysteresis voltage may vary.
∗3) If Vup and V_{DD} are connected, the voltage dropdown caused by Rup, may cause difference in the hysteresis voltage.
∗4) If the value of Ra, Rb and C are set excessively large, the delay of the start-up may become too long.

Window Comparator Circuit
(Nch Open Drain Output)





Over-charge Preventing Circuit



RICOH

TECHNICAL NOTES

When connecting resistors to the device's input pin

When connecting a resistor (R1) to an input of this device, the input voltage decreases by [Device's Consumption Current] x [Resistance Value] only. And, the cross conduction current*[1], which occurs when changing from the detecting state to the release state, is decreased the input voltage by [Cross Conduction Current] x [Resistance Value] only. And then, this device will enter the re-detecting state if the input voltage reduction is larger than the difference between the detector voltage and the released voltage.

When the input resistance value is large and the VDD is gone up at mildly in the vicinity of the released voltage, repeating the above operation may result in the occurrence of output.

As shown in Figure A/B, set R1 to become 100kΩ or less as a guide, and connect C_{IN} of 0.1μF and more to between the input pin and GND. Besides, make evaluations including temperature properties under the actual usage condition, with using the evaluation board like this way. As result, make sure that the cross conduction current has no problem.

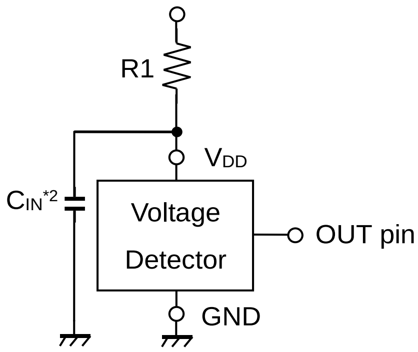


Figure A

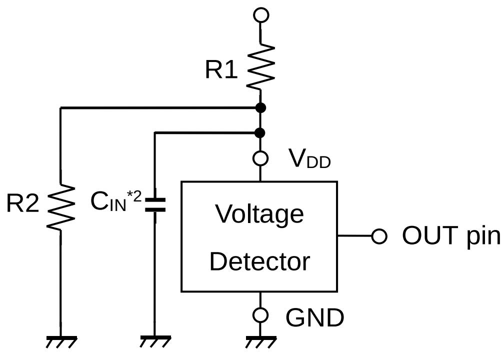


Figure B

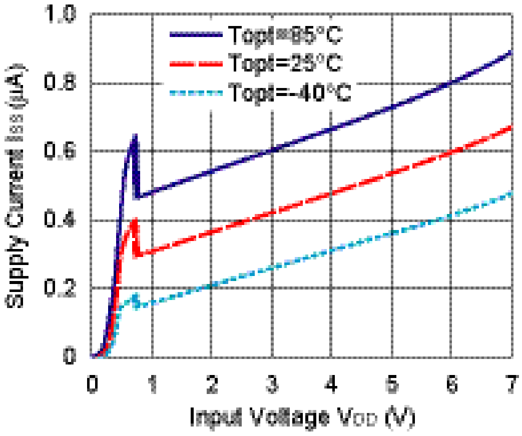
*[1] In the CMOS output type, a charging current for OUT pin is included.
*[2] Note the bias dependence of capacitors.

TYPICAL CHARACTERISTICS

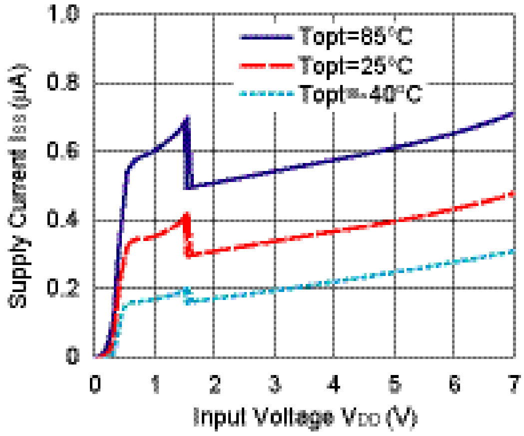
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Supply Current vs. Input Voltage

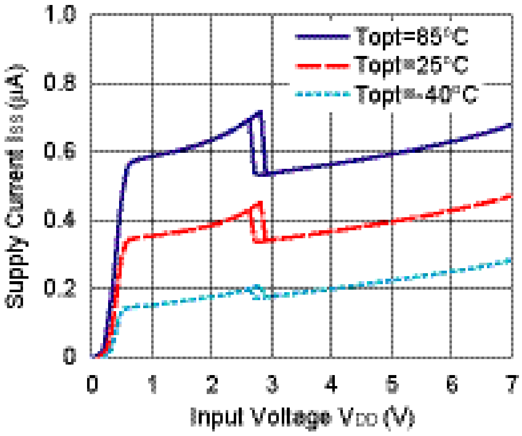
R3116x071A/C



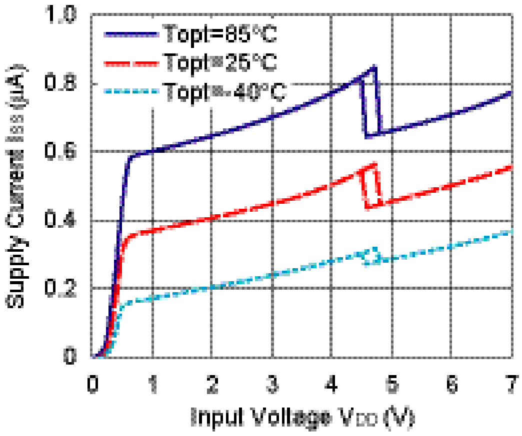
R3116x151A/C



R3116x271A/C

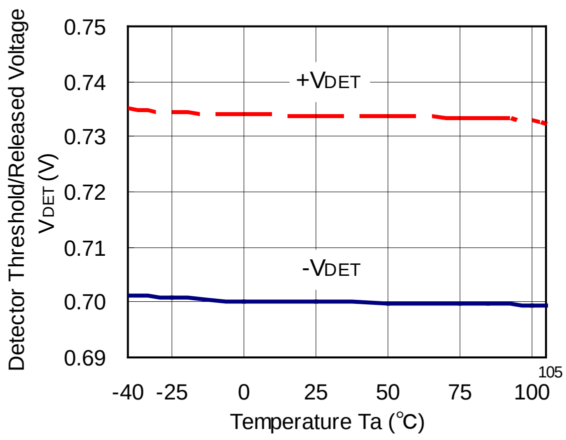


R3116x451A/C

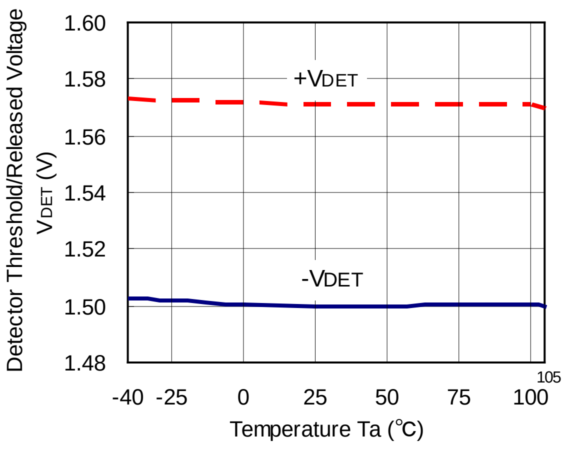


2) Detector Threshold vs. Temperature

R3116x071A/C



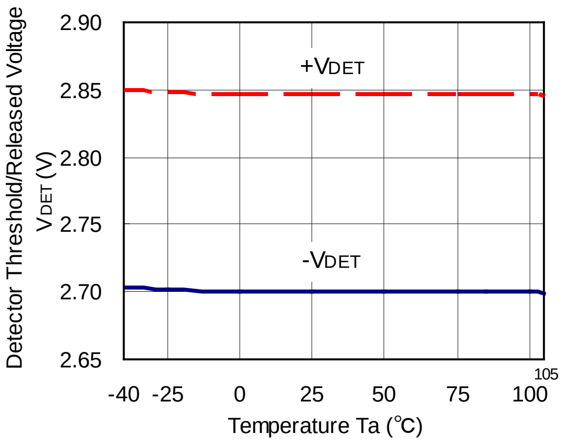
R3116x151A/C

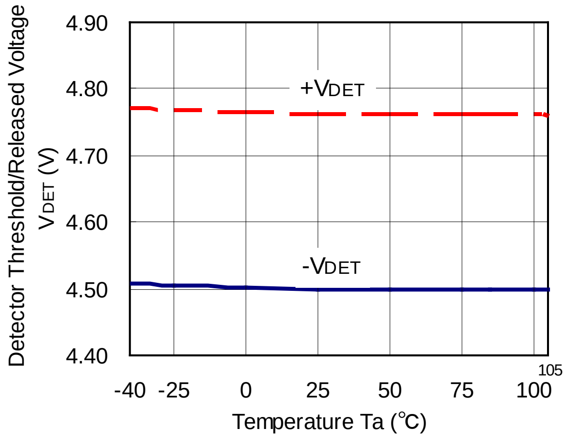


R3116x271A/C

R3116x451A/C

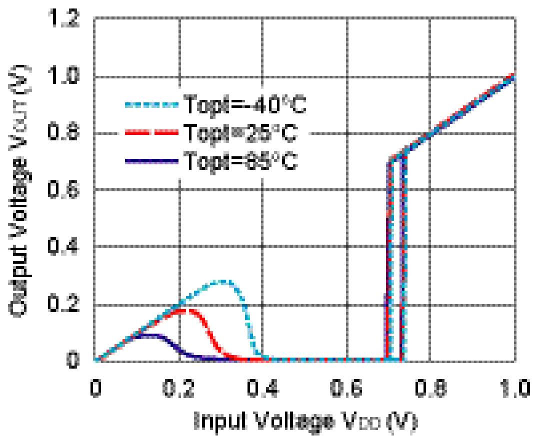
RICOH



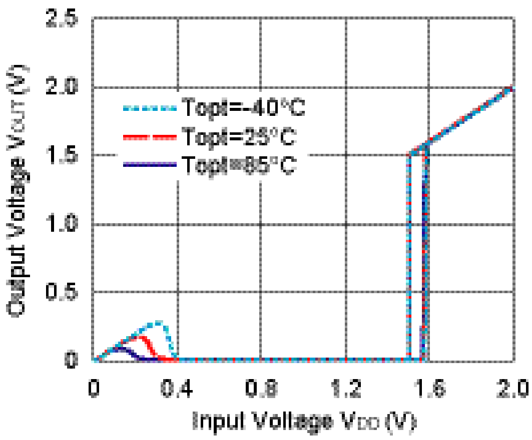


3) Output Voltage vs. Input Voltage

R3116x071C



R3116x151C



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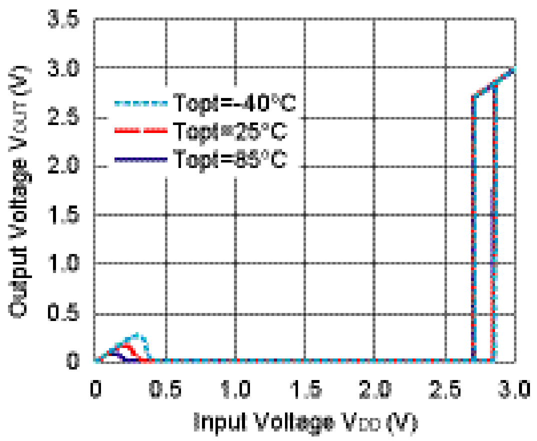

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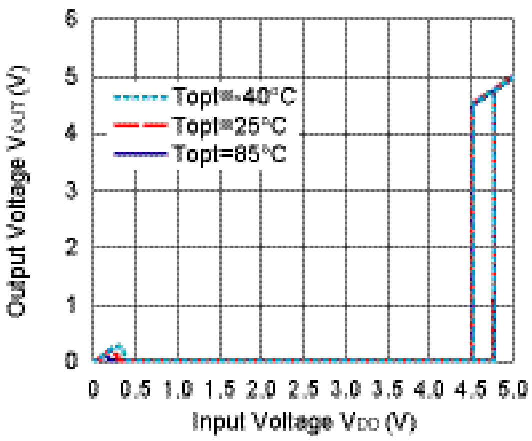
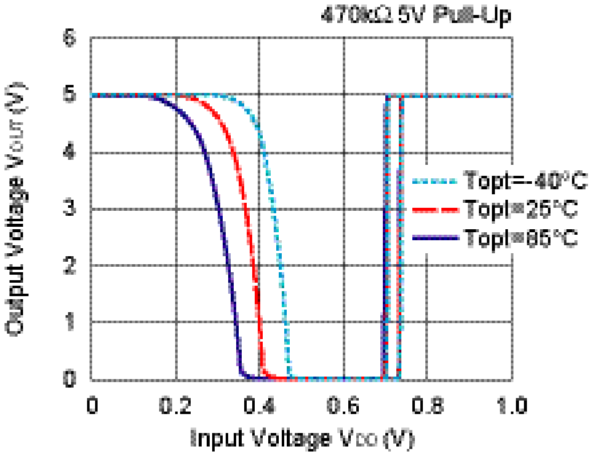
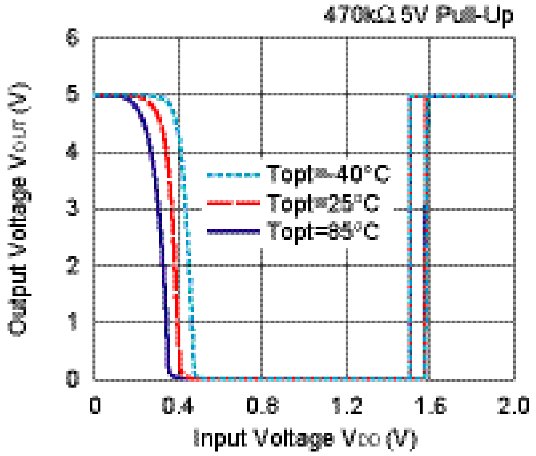


RICOH

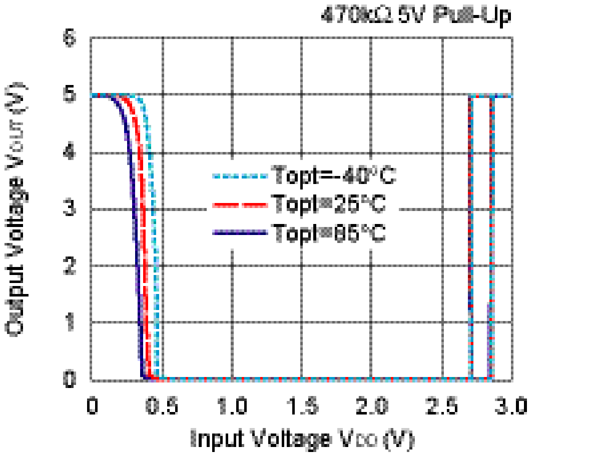
R3116x071A



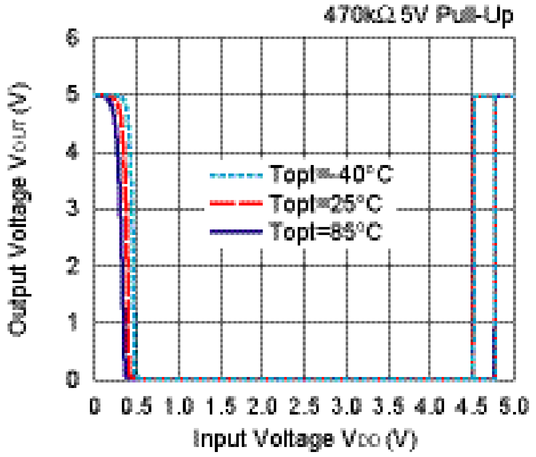
R3116x151A



R3116x271A

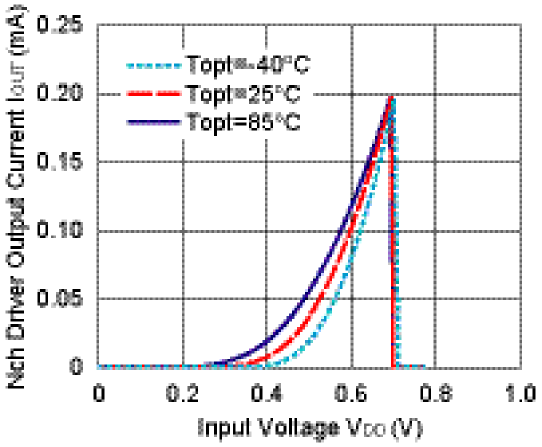


R3116x451A

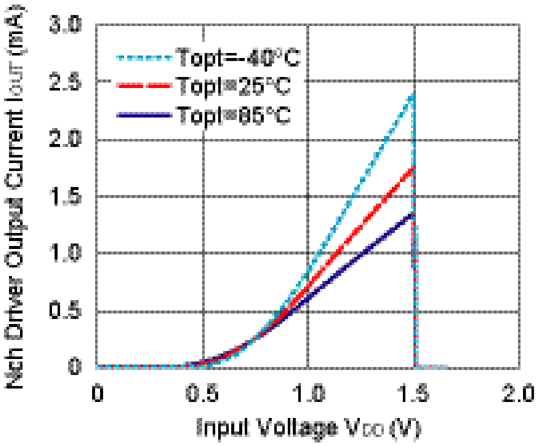


4) Nch Driver Output Current vs. Input Voltage (V_{DS}=0.5V)

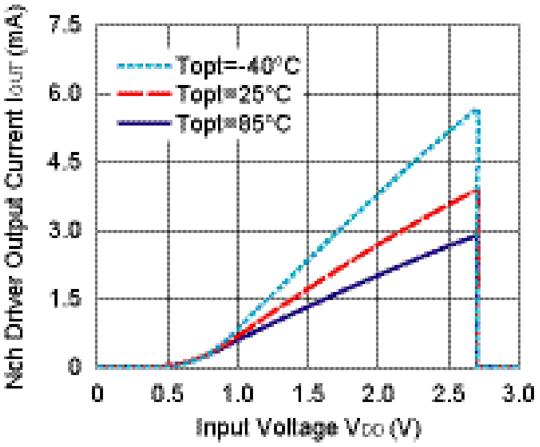
R3116x071A/C



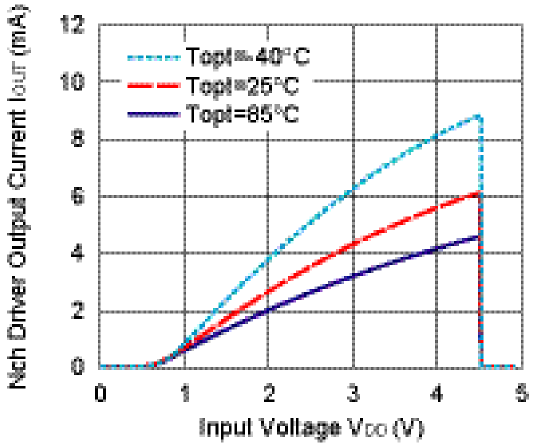
R3116x151A/C



R3116x271A/C

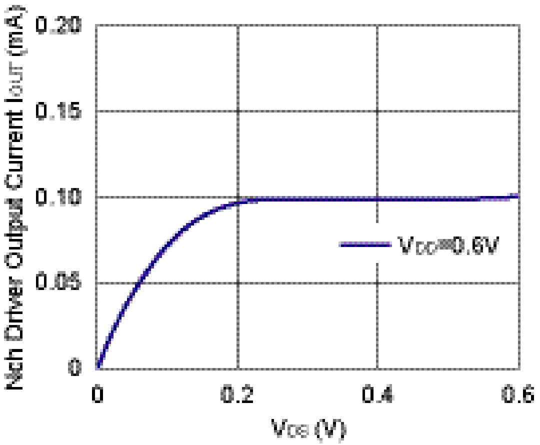


R3116x451A/C

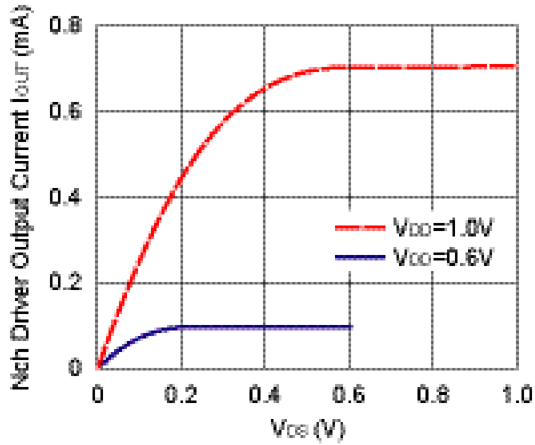


5) Nch Driver Output Current vs. V_{DS}

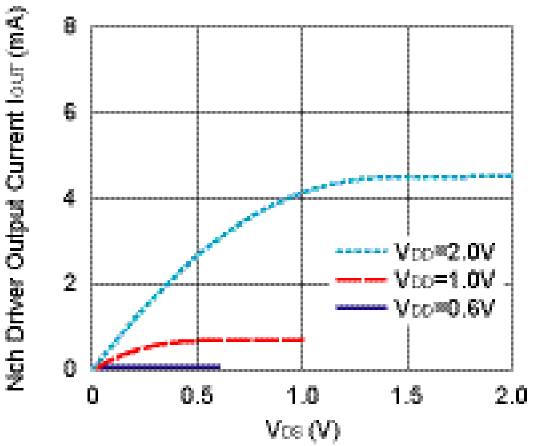
R3116x071A/C



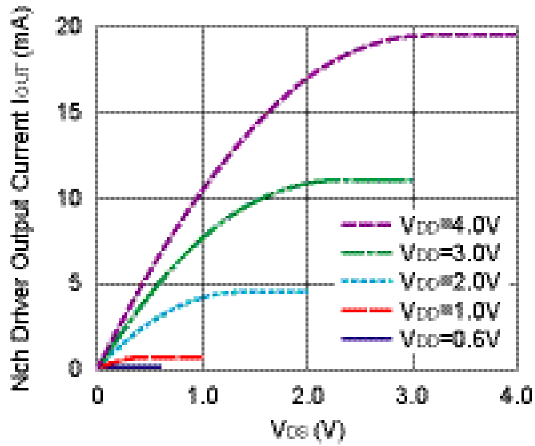
R3116x151A/C



R3116x271A/C

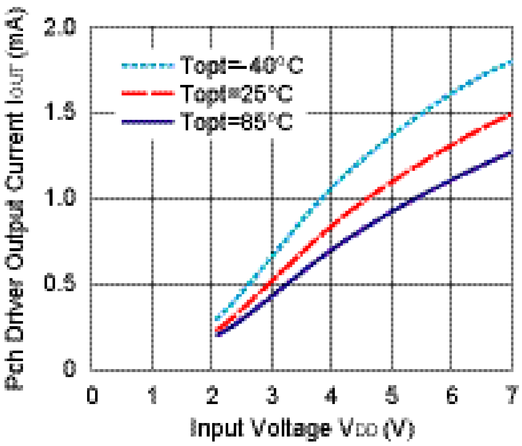


R3116x451A/C



6) Pch Driver Output Current vs. Input Voltage (V_{DS}=–2.1V)

R3116x071C



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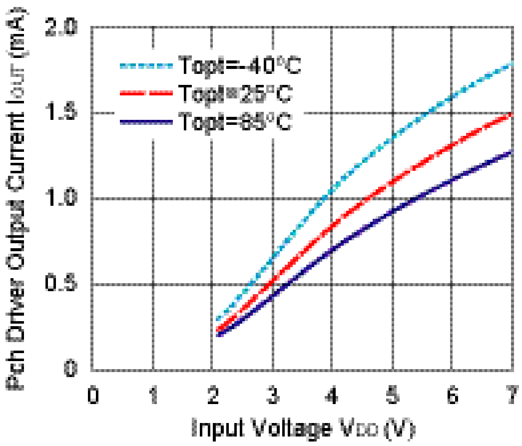

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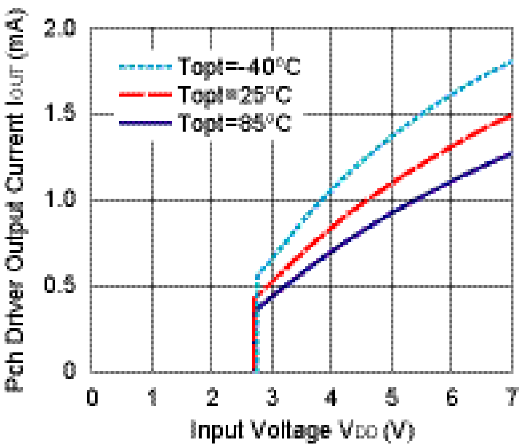

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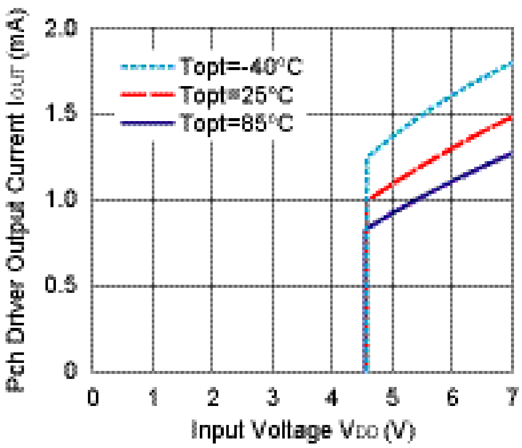
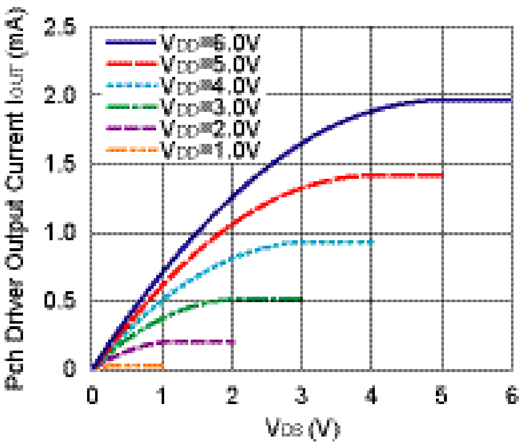


7) Pch Driver Output Current vs. V_{DS}

R3116x071C



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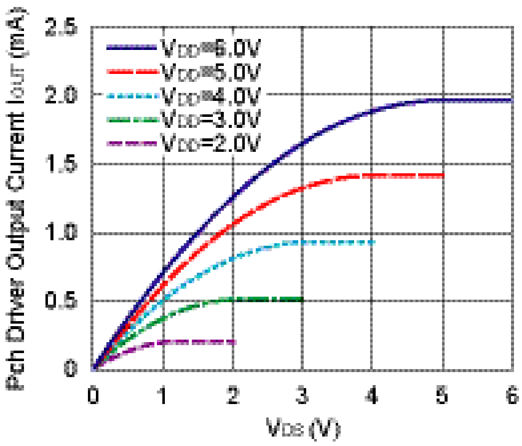

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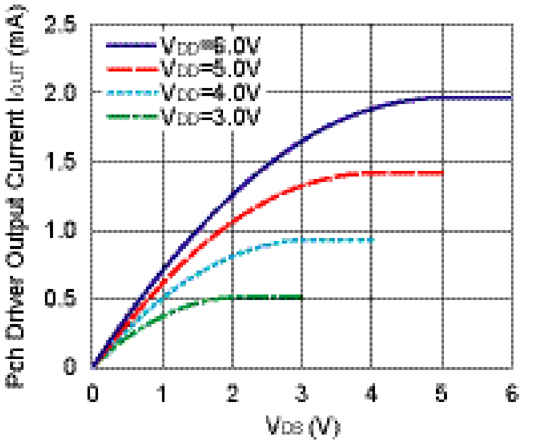

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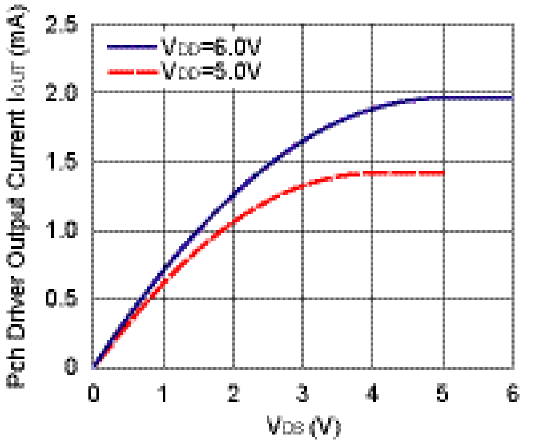
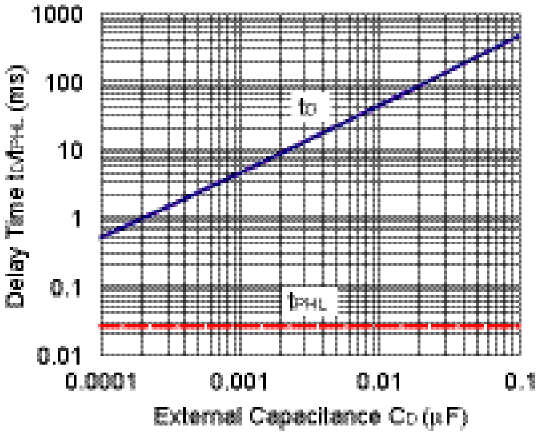
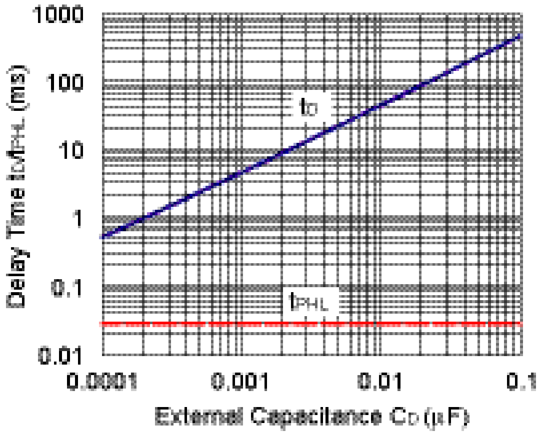


8) Output Delay Time vs. External Capacitance

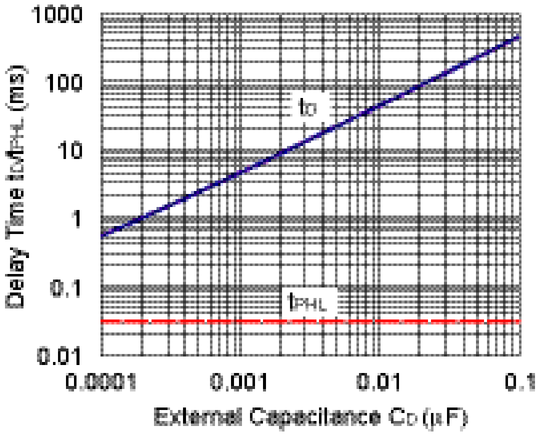
R3116x071A/C



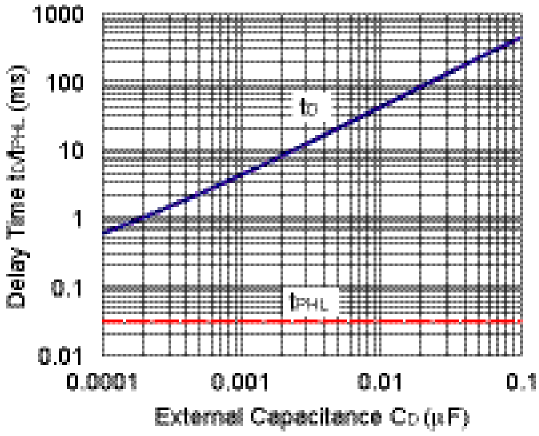
R3116x151A/C



R3116x271A/C

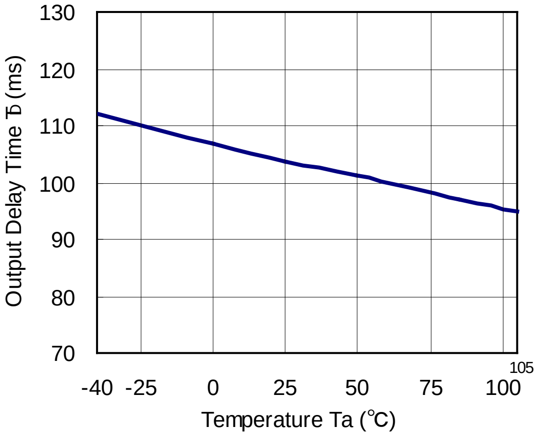


R3116x451A/C

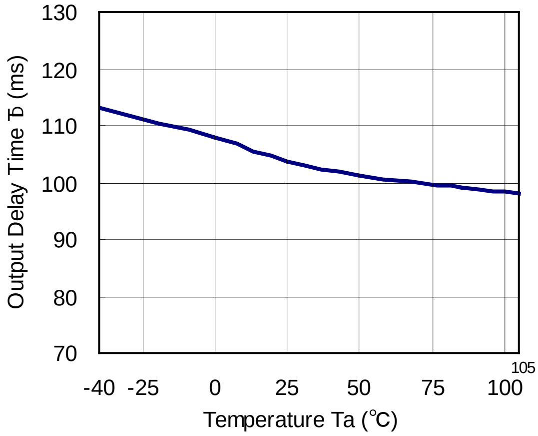


9) Output Delay Time vs. Temperature (C_D=22nF)

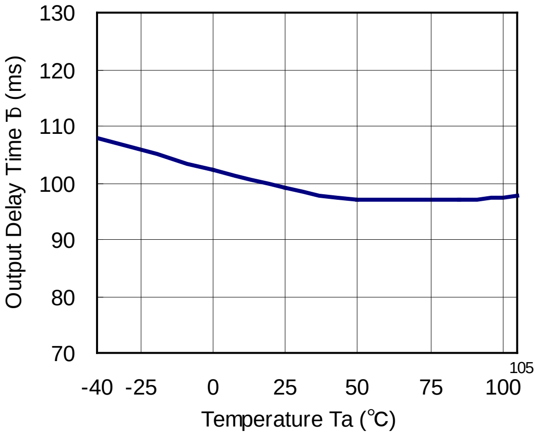
R3116x071A/C



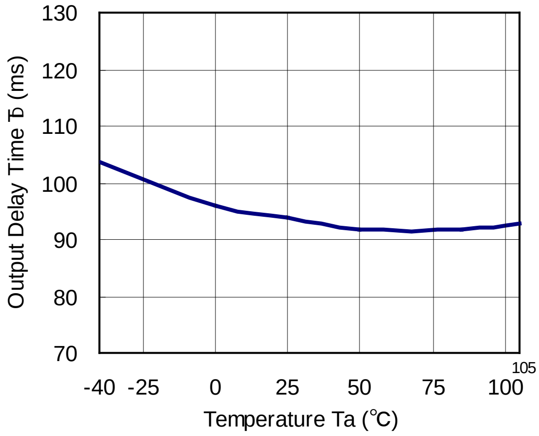
R3116x151A/C



R3116x271A/C



R3116x451A/C



Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

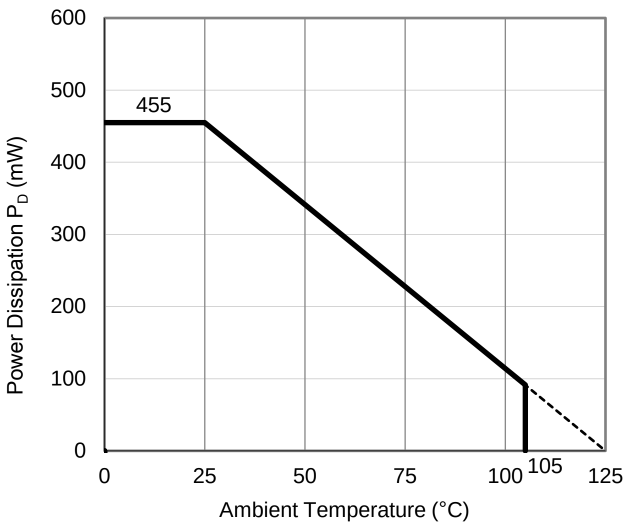
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layers (First and Forth Layers): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.85 mm × 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

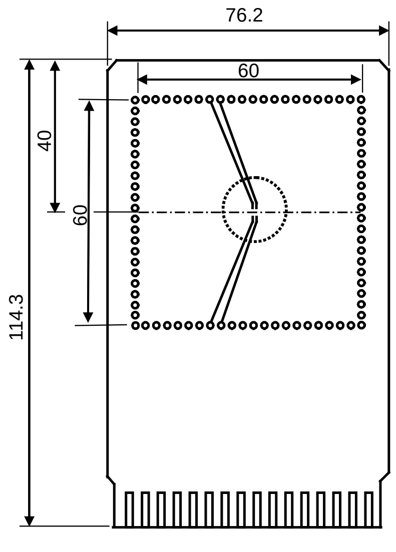
Item	Measurement Result
Power Dissipation	455 mW
Thermal Resistance (θja)	θja = 220°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 68°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



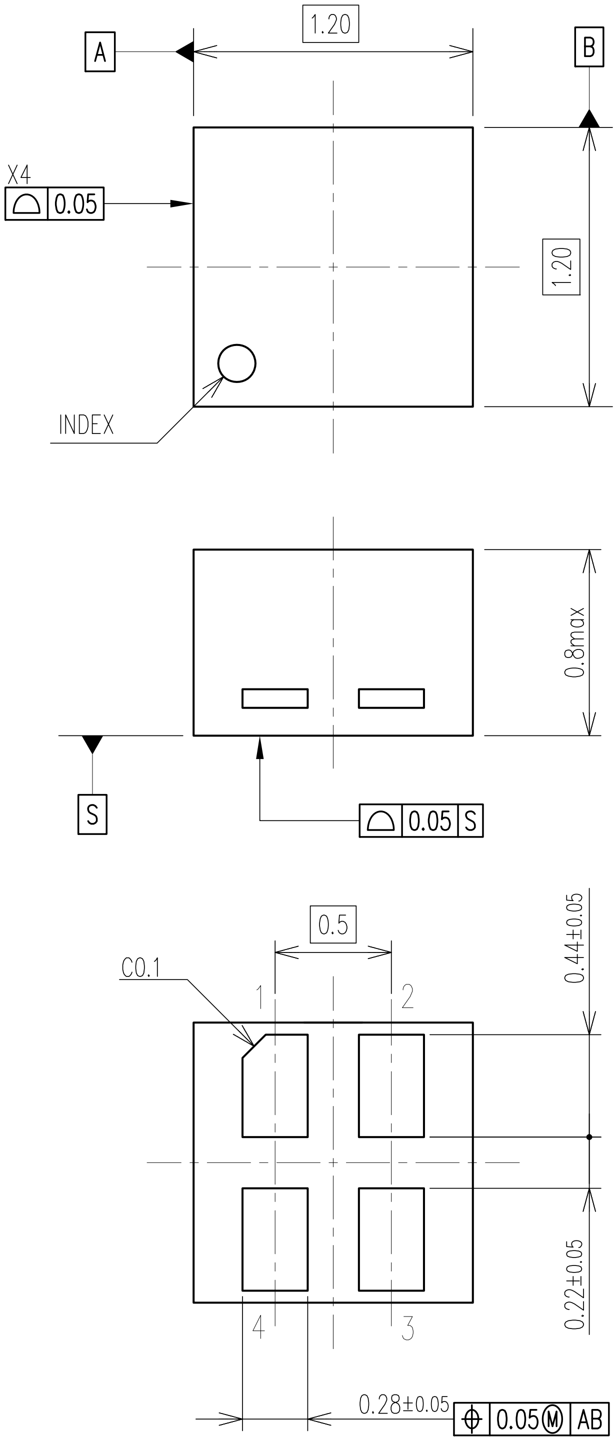
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH

Ver. A



DFN1212-4 Package Dimensions (Unit: mm)

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

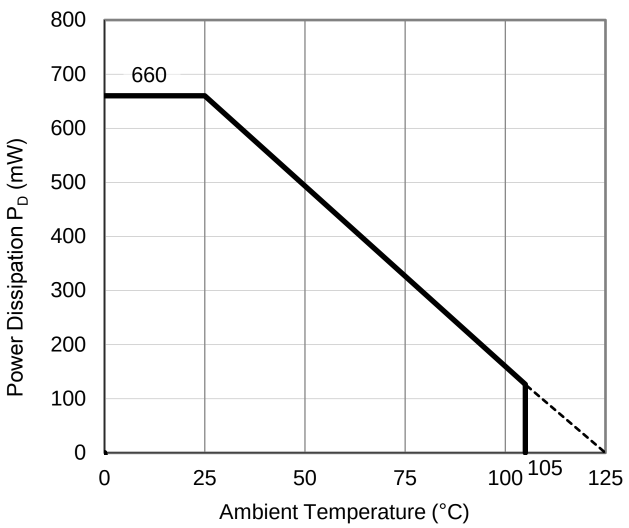
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 7 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

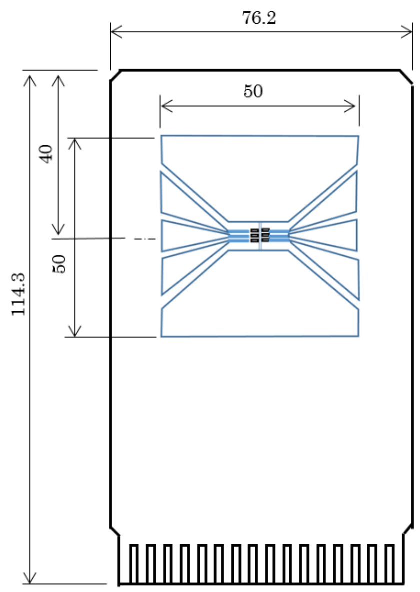
Item	Measurement Result
Power Dissipation	660 mW
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

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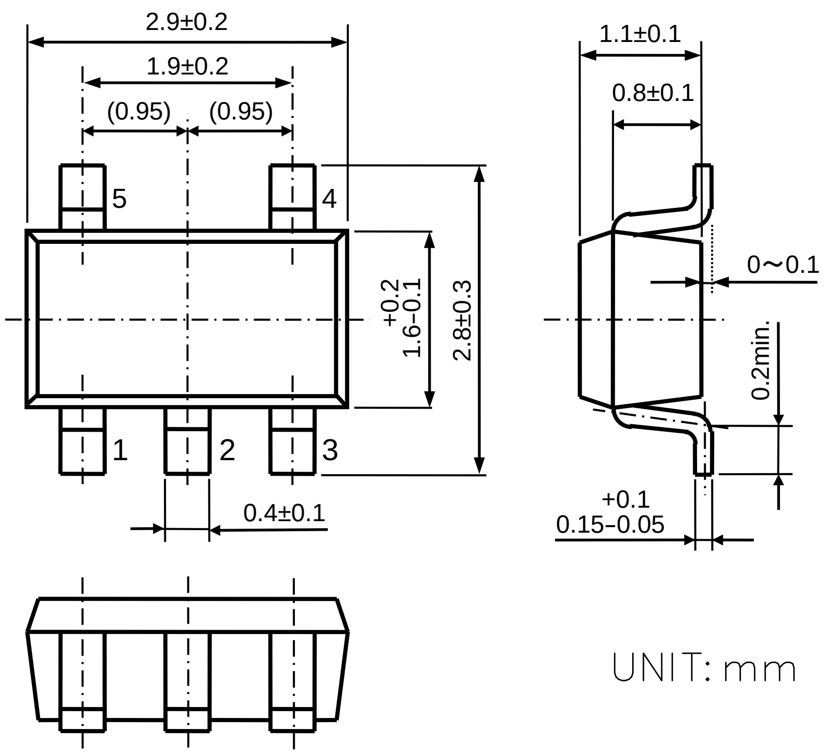

SOT-23-5 Package Dimensions

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